CLAIMS

What is claimed is:

1. A method for designing at least one mask for manufacturing an integrated circuit comprising:

generating a schematic for the integrated circuit, the integrated circuit comprising a set of transistors;

entering data representing each transistor of the set into a computer-aided design system;

identifying a first subset of the set of transistors wherein the transistors of the first subset are expected to be subject to voltage levels beyond the bounds of a power rail and a ground rail of the integrated circuit during normal operation;

designating, in the computer-aided design system, robust geometries for the transistors of the first subset;

and

operating the computer-aided design system to generate the at least one mask.

2. The method of claim 1 further comprising:

identifying a second subset of the set of transistors, wherein the transistors of the second subset are input-output transistors

and

designating, in the computer aided design system, robust geometries for the transistors of the second subset.

3. An integrated circuit comprising:

a semiconductor die formed using at least one mask designed by the acts of:

generating a schematic for the integrated circuit, the integrated circuit comprising a set of transistors;

entering data representing each transistor of the set into a computer-aided design system;

identifying a first subset of the set of transistors wherein the transistors of the first subset are expected to be subject to voltage levels beyond the bounds of a power rail and a ground rail of the integrated circuit during normal operation;

designating, in the computer-aided design system, robust geometries for the transistors of the first subset, such that the set of data may be used to generate a plurality of masks for lithography of features having mutually different minimum line widths.

4. The integrated circuit claim 3 wherein:

the at least one mask is designed by acts further comprising:

identifying a second subset of the set of transistors, wherein the transistors of the second subset are input-output transistors

and

designating, in the computer aided design system, robust geometries for the transistors of the second subset.

5. The integrated circuit claim 3 wherein:

the integrated circuit implements a radio frequency circuit.

6. The integrated circuit claim 1 wherein:

the integrated circuit implements a hybrid circuit.

7. The integrated circuit claim 3 wherein:

the semiconductor die comprises metal-oxide transistors is formed using lithography.

8. A method for designing a plurality of masks for manufacturing an integrated circuit migrated across a plurality of feature size technologies, each mask associated with a respective feature size technology, the method comprising:

generating a schematic for the integrated circuit, the integrated circuit comprising a set of transistors;

entering data representing each transistor of the set into a computer-aided design system;

identifying a first subset of the set of transistors wherein the transistors of the first subset are expected to be subject to voltage levels beyond the bounds of a power rail and a ground rail of the integrated circuit during normal operation;

designating, in the computer-aided design system robust geometries for the transistors of the first subset;

and

operating the computer aided design system to generate a first mask associated with a first feature size technology and a second mask associated with a second feature size technology, wherein a respective geometry of each transistor of the first subset is the same for both the first mask and the second mask.